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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/550,282	04/14/2000	Sung-Il Park	1607-0211P	9574

2292 7590 05/01/2006

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EXAMINER	
QI, ZHI QIANG	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 05/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/550,282	PARK ET AL.	
	Examiner	Art Unit	
	Mike Qi	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,11-15,17 and 19-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,11-15,17 and 19-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The Final Office Action mailed on Sep. 22, 2005 is vacated and prosecution is reopened.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5-6,11-15, and 20-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,259,200 (Morita et al) in view of US 5,870,157 (Shimada et al) and US 6,172,728 B1 (Hiraishi).

Regarding claims 1, 5-6,15 and 20-22, **Morita** discloses (col.5, lines 59 – col.6, line 65; Figs.5-6) that a liquid crystal display device comprising:

- gate line (43) formed on a transparent substrate (1), and gate electrode (G) of the TFT (3) to be connected with the gate line (43) on the transparent substrate (1);
- data lines (signal line 10) crossing the gate line (43) and formed on the transparent substrate (1); and the data line (10), the source electrode and the drain electrode over the transparent substrate (1); and the source electrode and the drain electrode being respectively disposed in source

area (7) and drain area (8); and the source electrode being connected with the data line (10) through contact hole (S);

- gate insulating layer (4a,4b) electrically insulating the data line (43) from the gate line (10) and gate electrode (G); and over the gate line (43) and the gate electrode (G), i. e., forming an insulating layer electrically insulating the gate line and the gate electrode;
- semiconductor layer (2) over the gate electrode (G);
- thin film transistor (TFT) (3) formed at an intersection of the gate line (43) and the data line (10), and connected to the gate line (43) and the data line (10), and the TFT being disposed in an area having a channel area (between the source area and the drain area), a source area (7) (first portion of the semiconductor layer 2) and a drain area (8) (second portion of the semiconductor layer 2); and the TFT (3) having gate electrode, source electrode and drain electrode;
- passivation layer (planarization film 12 functions as passivation layer (col.4, lines 31-32) formed over the TFT (3); and having contact hole exposing the drain electrode over the transparent substrate (1);
- pixel electrode (14) having portions formed on the surface of the passivation layer(planarization film 12 functions as a passivation layer), but not over the TFT (3); and connected to the drain electrode via the contact hole;
- upper substrate (60) located above the pixel electrode (14).

Morita does not expressly discloses that:

1) a low reflective layer covers at least a portion of the gate line or a portion of the data line or formed on the first portion (source area), the second portion (drain area), the channel region to shield the light;

2) no black layer or light shielding layer between the pixel electrode and the upper substrate and above the low reflective layer.

Shimada teaches (col.4, line 39 – col.5, line 54; Figs.1-3) that no black matrix (black layer) is provided on the counter substrate (upper substrate) (19), and the line (10) (a source or gate line) on the active matrix substrate (18) are used as a light-blocking pattern for blocking light (because the line 10 having function to block light, so that the material of the line 10 having function as a low reflectance and the line 10 should be a low reflective layer) so as to improve the aperture ratio and to realize high display quality (see col.5, lines 37-40).

Shimada further teaches (col.5, lines 47-54; Figs.1-3) that the surface of the source lines (23) and the gate lines (22) on the active matrix substrate (18) are formed of chromium oxide (CrOx) so as to reduce the reflectance of the surfaces and improve the effectiveness of light blocking (see col.2, lines 39-42). Therefore, the skilled in the art would be benefit from the teachings to use such low reflective layer (such as CrOx) covering the gate line or the data line or the source area or the drain area or the channel region so as to reduce the reflectance of the surfaces and improve the effectiveness of light blocking (to shield the light).

Concerning claims 5-6 and 20-21, the low reflective layer is formed of CrOx and having a light reflectivity of 3% or less, that is the property of the material (CrOx), and the same material has the same property, and that would have been at least obvious.

Hiraishi further teaches (col.6, lines 34-37) that the display quality is enhanced by providing a low-reflective film preferably made of chromium oxide (CrOx) on the gate lines and the source lines, i.e., a low reflective layer covering the gate line or the data line or the source area or the drain area or the channel region so as to reduce the reflectance of the surfaces that is to shield the light and to enhance the display quality.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the liquid crystal display of Morita with the teachings of no black matrix on the upper substrate and using a low reflective layer covering the gate line or the data line as taught by Shimada and Hiraishi, since the skilled in the art would be motivated for improving the aperture ratio and achieving high display quality and improving the effectiveness of light blocking (see Shimada col.5, lines 37-40) and enhancing the display quality (see Hiraishi col.6, lines 34-37).

Regarding claim 11, Morita discloses (col.5, lines 59 – col.6, line 65; Figs.5-6) that the passivation layer (planarization film 12 functions as passivation layer) formed over the gate line (gate electrode G connected to the gate line 43), the data line (the source electrode connected to the signal line 10), the low reflective layer (because low reflective layer as the covering surface of the gate line or the data line); and the pixel electrode (14) formed on the passivation layer (12); and the pixel electrode (14) is connected to the TFT via a contact hole in the passivation layer (12).

Regarding claims 14 and 25, Morita discloses (col.7, lines 14-25; Fig.6) that a color filter (63) is formed on the color filter substrate (60); and liquid crystal (50) sealed between the color filter substrate (60) and transparent substrate (1).

Regarding claims 12-13 and 23-24, Morita, Shimada and Hiraishi teach the invention set forth above.

Shimada further teaches (col.3, lines 60-63) that the pixel electrodes overlap the scanning and signal lines (gate line and date line as shown in Fig.1), the aperture ratio of the liquid crystal display device is improved.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the liquid crystal display of Morita, Shimada and Hiraishi with the teachings of the pixel electrode overlap a portion of data line or gate line as taught by Shimada, since the skilled in the art would be motivated for improving the aperture ratio (see Shimada col.3, lines 60-63).

3. Claims 3-4, 17, 19 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morita, Shimada and Hiraishi as applied to claims 1, 5-6,11-15, and 20-25 above, and further in view of US 6,172,723 (Inoue et al).

Regarding claims 3-4, 17, 19 and 26, Morita, Shimada and Hiraishi teach the invention set forth above.

Morita further discloses (col.5, lines 59 – col.6, line 65; Figs.5-6) that the thin film transistor (TFT) includes:

- thin film transistor having gate electrode (G), source electrode (S) and drain electrode (D);

- gate electrode (G) connected to the gate line (43); and the gate electrode (G) being covered with the channel region (between the source area 7 and the drain area 8);
- source electrode is connected to the data line (signal line 10), drain electrode is connected to the pixel electrode (14); and drain electrode connected to the drain line that would be an obvious variation as the source electrode connected to the data line for transferring data signal.

Shimada further teaches (col.5, lines 47-54; Figs.1-3) that the surface of the source lines (23) and the gate lines (22) on the active matrix substrate (18) are formed of chromium oxide (CrOx) so as to reduce the reflectance of the surfaces and improve the effectiveness of light blocking (see col.2, lines 39-42). Therefore, the skilled in the art would be benefit from the teachings to use such low reflective layer (such as CrOx) covering the gate line or the data line so as to reduce the reflectance of the surfaces and improve the effectiveness of light blocking (to shield the light). Even though the gate line and data line are not gate electrode or source/drain electrode (gate line and data line are the extension of the gate electrode and source/drain electrode), forming a low reflective layer on the gate electrode and on the source/drain electrode that also is forming a low reflective layer on a metal (conductive) layer that would be an obvious variation so as to enhancing the display quality. Especially, as a generally available knowledge, for the reason to protect the thin film transistor, because the light passing through the thin film transistor would cause malfunction. Such that the skilled in the art would be benefit from the teachings of using a low reflective layer formed on the gate

electrode and formed on the source and drain electrode to protect the thin film transistor.

As evidence, Inoue teaches (col.11, lines 34-50) that depositing a low reflection conductive material on a high reflection electrode (such as gate electrode, source electrode or drain electrode). Such that forming a low reflective layer on a metal (conductive) layer (such the electrodes of the thin film transistor) that would be an obvious variation so as to enhancing the display quality and protecting the thin film transistor.

Therefore, it would have been obvious to those skilled in the art at the time the invention was made to modify the liquid crystal display of Morita, Shimada and Hiraishi with the teachings of forming a low reflective layer on a high reflection electrode as taught by Inoue, since the skilled in the art would be motivated for enhancing the image display quality and protecting the thin film transistor.

Response to Arguments

4. Applicant's arguments with respect to claims 1, 3-6,11-15,17, and 19-26 have been considered but are moot in view of the new ground(s) of rejection.

The reference Shimada teaches (col.4, line 39 – col.5, line 54; Figs.1-3) that no black matrix (black layer) is provided on the counter substrate (upper substrate) (19), and the line (10) (a source or gate line) on the active matrix substrate (18) are used as a light-blocking pattern for blocking light. Shimada further teaches (col.5, lines 47-54; Figs.1-3) that the surface of the source lines (23) and the gate lines (22) on the active

matrix substrate (18) are formed of chromium oxide (CrOx) so as to reduce the reflectance of the surfaces and improve the effectiveness of light blocking (see col.2, lines 39-42).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mike Qi whose telephone number is (571) 272-2299. The examiner can normally be reached on M-T 8:00 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ZQQ

Mike Qi
Patent examiner
April 19, 2006